CLAIMS

WHAT IS CLAIMED:

1. A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a strained surface layer on a surface of said substrate by implanting ions of at least one heavy inert material through said surface of said substrate; and

forming at least one gate structure above said strained surface layer.

2. The method of claim 1, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof, are implanted.

3. The method of claim 1, wherein the implanting energy is selected in the range of approximately 10-100 keV.

4. The method of claim 1, wherein the implanting dose is selected in the range of approximately $10^{13}/cm^2 - 10^{16}/cm^2$.

5. The method of claim 1, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid grid restoration of the substrate.

6. The method of claim 1, wherein said substrate comprises one of silicon and germanium or a combination thereof.

7. The method of claim 1, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

8. A method of forming at least one field effect transistor on a semiconductive substrate, the method comprising

forming an insulating film on a surface of said substrate;

generating a strained surface layer at the interface of said insulating film and said substrate by implanting ions comprised of at least one heavy inert material through the gate insulating film into said substrate; and

forming a gate insulating structure.

9. The method of claim 8, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof are implanted.

10. The method of claim 8, wherein the implanting energy is in the range of approximately 20-200 keV.

11. The method of claim 8, wherein the implanting dose is in the range of approximately $10^{13}/cm^2 - 10^{16}/cm^2$.

12. The method of claim 8, wherein a thermal budget is adjusted to substantially avoid the grid restoration of said substrate.

13. The method of claim 8, wherein said substrate comprises one of silicon and germanium or a combination thereof.

14. The method of claim 8, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

15. The method of claim 8, wherein said insulating film comprises oxide, the method further comprising patterning said insulating film to form said gate insulating film and forming a gate polysilicon structure on said gate insulating film.

16. The method of claim 8, further comprising removing said insulating film after generating said strained layer, forming a gate insulating layer and patterning said gate insulating layer to form said insulating gate structure.